Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Original) A method of co-processing, comprising:

connecting an interface of a first processor to an interface of a second processor using a bus, the interface of the second processor being configurable to place the second processor in a slave processing mode or a master processing mode; and

sending a task from the first processor to the second processor through the bus, the task comprises an instruction that places the second processor in a slave processing mode.

2. (Original) The method of claim 1, wherein the task further comprises an instruction that places the second processor in a master processing mode.

3. (Original) The method of claim 1, further comprising:

sending data from the second processor to the first processor based on the task received from the first processor

4. (Original) The method of claim 1, wherein the interface of the first processor includes a first quad data rate (QDR) interface and the interface of the second processor includes a second QDR interface.

5. (Original) The method of claim 1, wherein the interface of the first processor includes a first quad data rate (QDR) interface and the interface of the second processor includes a first media switch fabric (MSF) interface.

6. (Original) The method of claim 5, further comprising connecting a second QDR interface of the second processor to a second MSF interface of a third processor using a second bus.

7. (Original) The method of claim 6, wherein the first, second and third processors are processors in a plurality of processors and the method further comprises:

connecting the plurality of processors successively in a chain with the first processor at one end of the chain and a last processor at the opposite end of the chain from the first processor, each of the plurality processors having an MSF interface and a QDR interface; and

connecting the QDR interface of the last processor to an external memory.

8. (Currently amended) The method of claim 7, further comprising:

sending [[a]] the task from [[a]] the first processor to the last processor;

executing the task; and

sending a result to the first processor.

9. (Original) The method of claim 6, wherein the first, second and third processors are processors in a plurality of processors and the method further comprises:

connecting the plurality of processors successively in a chain with the first processor at one end of the chain and a last processor at the opposite end of the chain from the first processor, each of the plurality processors having an MSF interface and a QDR interface; and

connecting the QDR interface of the last processor to the MSF interface of the first processor.

10. (Original) The method of claim 9, further comprising:

sending instructions from the first processor to the last processor;

executing the instructions; and

sending a result to the first processor.

11. (Original) The method of claim 1, wherein the first processor has a first processing speed and the second processor has a second processing speed, the first processing speed is greater than the second processing speed.

12. (Currently amended) An apparatus comprising:

a first processor having an interface connected to an interface of a second processor using a bus, the interface of the first processor being configurable to place the first processor in a slave processing mode or a master processing mode; and

circuitry, for co-processing, to:

receive a task from the second processor through the bus, the task comprises an instruction that places the first processor in a slave processing mode.

13. (Original) The apparatus of claim 12, wherein the task further comprises an instruction that places the first processor in a master processing mode.

14. (Original) The apparatus of claim 12, further comprising circuitry to:

send data from the first processor to the second processor based on the task received from the second processor.

15. (Original) The apparatus of claim 12 wherein the interface of the first processor includes a quad data rate (QDR) interface and the interface of the second processor includes a QDR interface.

16. (Original) The apparatus of claim 12, wherein the interface of the second processor includes a quad data rate (QDR) interface and the interface of the first processor includes a media switch fabric (MSF) interface.

17. (Original) The apparatus of claim 16, wherein a QDR interface of the first processor is connected to a MSF interface of a third processor using a second bus.

18. (Original) The apparatus of claim 17, wherein the first, second and third processors are processors in a plurality of processors successively coupled in a chain with the first processor at one end of the chain and a last processor at the opposite end of the chain from the first processor, each of the plurality processors having an MSF interface and a QDR interface, the QDR interface of the last processor is connected to an external memory.

19. (Currently amended) The apparatus of claim 18, further comprising circuitry to:
send [[a]] the task from the second processor to the last processor;
execute the task; and
send a result to the second processor.

20. (Original) The apparatus of claim 17, wherein the first, second and third processors are processors in a plurality of processors successively coupled in a chain with the first processor at one end of the chain and a last processor at the opposite end of the chain from the first processor, each of the plurality processors having an MSF interface and a QDR interface, the QDR interface of the last processor is connected to the MSF interface of the ~~second~~ first processor.

21. (Original) The apparatus of claim 20, further comprising circuitry to:

send instructions from the second processor to the last processor;

execute the instructions; and

send a result to the second processor.

22. (Currently amended) An article comprising a machine-readable storage device ~~medium~~ that stores executable instructions for co-processing, the instructions causing a machine to:

send a task from an interface of a first processor to an interface of a second processor through a bus, the interface of the second processor being configurable to place the second processor in a slave processing mode or a master processing mode, the task comprises an instruction that places the second processor in a slave processing mode.

23. (Original) The article of claim 22, wherein the task further comprises an instruction that places the second processor in a master processing mode.

24. (Original) The article of claim 22, further comprising instructions causing a machine to:

send data from the second processor to the first processor based on the task received from the first processor

25. (Original) The article of claim 22 wherein the interface of the first processor includes a first quad data rate (QDR) interface and the interface of the second processor includes a second QDR interface.

26. (Original) The article of claim 22, wherein the interface of the first processor includes a first quad data rate (QDR) interface and the interface of the second processor includes a first media switch fabric (MSF) interface.

27. (Original) The article of claim 26, wherein a QDR interface of the second processor is connected to an MSF interface of a third processor using a second bus.

28. (Original) The article of claim 27, wherein the first, second and third processors are processors in a plurality of processors successively coupled in a chain with the first processor at one end of the chain and a last processor at the opposite end of the chain from the first processor, each of the plurality processors having an MSF interface and a QDR interface, the QDR interface of the last processor is connected to an external memory.

29. (Currently amended) The ~~apparatus~~ article of claim 28, further comprising instructions causing [[a]] the machine to:

send a task from [[a]] the first processor to the last processor;

execute the task; and

send a result to the first processor.

30. (Currently amended) The ~~method~~ article of claim 27, wherein the first, second and third processors are processors in a plurality of processors successively coupled in a chain with the first processor at one end of the chain and a last processor at the opposite end of the chain from the first processor, each of the plurality processors having an MSF interface and a QDR interface, the QDR interface of the last processor is connected to the MSF interface of the ~~second~~ first processor.

31. (Currently amended) The ~~method~~ article of claim 30, further comprising instructions causing [[a]] the machine to:

send instructions from the first processor to the last processor;

execute the instructions; and

send a result to the first processor.

32. (Original) A network router, comprising:

a network co-processing system, the network co-processing system comprising:

a first processor having an interface; ~~and~~

a second processor having an interface connected to the interface of the first processor by a bus, the interface of the second processor being configurable to place the second processor in a slave processing mode or a master processing ~~mode.~~ mode;

an input line connecting the network co-processing system to a first network; and

an output line connecting the network co-processing system to a second network.

33. (Original) The router of claim 32 wherein the interface of the first processor includes a first quad data rate (QDR) interface and the interface of the second processor includes a second QDR interface.

34. (Original) The router of claim 32, wherein the interface of the first processor includes a first quad data rate (QDR) interface and the interface of the second processor includes a media switch fabric (MSF) interface.

35. (Original) The router of claim 34, wherein a QDR interface of the second processor is connected to a MSF interface of a third processor using a second bus.

36. (New) The method of claim 1, wherein the interface of the second processor is configured to provide the task to the second processor when the second processor is in slave mode, and to send one of a result of the task and another task to the first processor when the second processor is in master mode.

37. (New) The apparatus of claim 12, wherein the interface of the first processor is configured to provide the task to the first processor when the first processor is in slave mode, and

to send one of a result of the task and another task to the second processor when the first processor is in master mode.

38. (New) The article of claim 22, wherein the interface of the second processor is configured to provide the task to the second processor when the second processor is in slave mode, and to send one of a result of the task and another task to the first processor when the second processor is in master mode.

39. (New) The router of claim 32, wherein the interface of the second processor is configured to provide a task to the second processor when the second processor is in slave mode, and to send one of a result of the task and another task to the first processor when the second processor is in master mode.